AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF THE CLAIMS:

Claims 1-61. (canceled)

62. (currently amended) A voltage level shifting circuit comprising:

a MOSFET which has either one of source/drain routes thereof connected to an input node to which an input voltage is supplied and has a predetermined voltage supplied to a gate thereof; and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit and allows a DC current component to flow therethrough,

wherein the voltage level shifting circuit obtains an output voltage from another source/drain route of the MOSFET,~~A voltage level shifting circuit according to claim 61,~~

wherein a capacitor is provided in parallel to the current source,

wherein the capacitor is a MOS capacitor which is configured to have a sufficiently large capacitance value with respect to a drain-source parasitic capacitance of the MOSFET,

wherein the current source is a depression type MOSFET which connects a gate and a source thereof to each other,

wherein the output voltage is supplied to an input of a first CMOS inverter circuit which is operated with a power source voltage smaller than the input voltage, and

wherein the predetermined voltage is the power source voltage.

Claims 63-64. (canceled)

65. (currently amended) A voltage level shifting circuit comprising:

a MOSFET which has either one of source/drain routes thereof connected to an input node to which an input voltage is supplied and has a predetermined voltage supplied to a gate thereof; and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit and allows a DC current component to flow therethrough,

wherein the voltage level shifting circuit obtains an output voltage from another source/drain route of the MOSFET, ~~A voltage level shifting circuit according to claim 61,~~

wherein a capacitor is provided in parallel to the current source,

wherein the capacitor is a MOS capacitor which is configured to have a sufficiently large capacitance value with respect to a drain-source parasitic capacitance of the MOSFET,

wherein the current source is a depression type MOSFET which connects a gate and a source thereof to each other,

wherein an output signal of the first CMOS inverter circuit is transmitted to an input of a second CMOS inverter circuit on a next stage, and

wherein an output signal of the second CMOS inverter circuit is fed back to a gate of the MOSFET which is provided between an input terminal of the second CMOS inverter circuit and a ground potential of the circuit thus allowing the first CMOS inverter circuit to possess a hysteresis transmission characteristic.

66. (previously presented) A voltage level shifting circuit according to claim 62, wherein

the MOSFET and the depression MOSFET are of an N-channel type, and

the input voltage and the power source voltage assume a positive voltages.

67. (currently amended) A voltage level shifting circuit comprising:

a MOSFET which has either one of source/drain routes thereof connected to an input node to which an input voltage is supplied and has a predetermined voltage supplied to a gate thereof;

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit and allows a DC current component to flow therethrough,

wherein the voltage level shifting circuit obtains an output voltage from another source/drain route of the MOSFET, ~~A voltage level shifting circuit according to claim 60,~~

wherein a capacitor is provided in parallel to the current source,

wherein the output voltage is supplied to an input part of an input circuit which is operated with a power source voltage smaller than the input voltage,

wherein the predetermined voltage is the power source voltage, and

wherein the input circuit includes a capacitive component in parallel to the capacitor.

Claims 68-75. (canceled)

76. (previously presented) A semiconductor integrated circuit device comprising:

a first switching element which controls a current for forming an output voltage by dropping an input voltage;

a terminal which allows the current to pass therethrough;

a second switching element which performs a switching operation which possess time in which the second switching element assumes an ON state when the first switching element assumes an OFF state thus controlling the current;

a first driving circuit which is operated by a first voltage corresponding to an input voltage thus driving the first switching element;

a second driving circuit which is operated by a second voltage thus driving the second switching element; and

a control logic circuit which is operated by the input voltage or a third voltage which is equal to or less than the second voltage, and forms a driving signal for the first

driving circuit and the second driving circuit by receiving control signals for the first switching element and the second switching element, wherein

the control logic circuit includes a first voltage level shifting circuit which shifts a voltage level of a driving signal for the first switching element in response to the third voltage and feedbacks the driving signal of the first switching element to an input of the second driving circuit, and a second voltage level shifting circuit which shifts a voltage level of a driving signal for the second switching element in response to the third voltage and feedbacks the driving signal for the second switching element to an input of the first driving circuit, and performs a switching control to prevent the first and second switching elements from simultaneously assuming an ON state, and

the first switching element, the terminal, the second switching element, the first driving circuit, the second driving circuit and the control logic circuit are sealed in one package.

77. (previously presented) A semiconductor integrated circuit device according to claim 76, wherein

the control signal is a PWM signal, and

the first and second voltage level shifting circuits respectively include

an input node to which the driving signal is supplied,

a MOSFET which has either one of source/drain routes thereof connected to the input node and has the third voltage supplied to the gate thereof, and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit and allows a DC current component to flow therethrough, wherein

the semiconductor integrated circuit device obtains a feedback signal which is generated by shifting a voltage level of the driving signal from another source/drain route of the MOSFET.

78. (previously presented) A semiconductor integrated circuit device according to claim 76, wherein

the control signal is a PWM signal,

the semiconductor integrated circuit device further includes a third voltage level shifting circuit,

the third voltage level shifting circuit is sealed in one package, and

the third voltage level shifting circuit includes

an input terminal to which an input signal for controlling an active/reactive (ON/OFF) state of the semiconductor integrated circuit device is supplied,

a MOSFET which has either one of the source/drain routes thereof connected to the input terminal and has the third voltage supplied to the gate thereof, and

a current source which is provided between another source/drain route of the MOSFET and a ground potential of a circuit and allows a DC current component to flow therethrough, and

the third voltage level shifting circuit obtains a control signal which is formed by shifting a voltage level of the input signal from another source/drain route of the MOSFET.

79. (previously presented) A semiconductor integrated circuit device according to claim 77, wherein

a capacitor is provided in parallel to the current source.

80. (previously presented) A semiconductor integrated circuit device according to claim 79, wherein

the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and

the current source is a depression type MOSFET which connects a gate and a source thereof to each other.

81. (previously presented) A semiconductor integrated circuit device according to claim 77, wherein

the feedback signal is transmitted to an input part of the control logic circuit which is operated with the third voltage smaller than the driving signal.

82. (previously presented) A semiconductor integrated circuit device according to claim 76, wherein

the current is a current which is made to flow in the inductor from a generating part of the input voltage to form the output voltage by the inductor and the capacity which is provided in series with the inductor.

Claims 83-89. (canceled)

90. (previously presented) A semiconductor integrated circuit device according to claim 76, wherein

the first switching element is formed on a first semiconductor substrate,

the second switching element is formed on a second semiconductor substrate, and

the first and second semiconductor substrates are sealed in one package.

91. (previously presented) A semiconductor integrated circuit device according to claim 90, wherein

the first driving circuit, the second driving circuit and the control logic circuit are formed on the third semiconductor substrate, and

the third semiconductor substrate is sealed in one package.

92. (previously presented) A semiconductor integrated circuit device according to claim 76, wherein

the first switching element, the second switching element, the first driving circuit, the second driving circuit and the control logic circuit are formed on one semiconductor substrate, and one semiconductor substrate is sealed in one package.

93. (previously presented) A semiconductor integrated circuit device according to claim 76, wherein

the semiconductor integrated circuit device includes

a first control terminal to which an input signal for controlling an active/reactive state of the semiconductor integrated circuit device is supplied,

a second control terminal which receives the PWM signal,

a power source terminal which supplies the second voltage, and

the second voltage is allowed to be set arbitrarily within a predetermined range by supplying a power source to the power source terminal from outside.

94. (previously presented) A semiconductor integrated circuit device according to claim 93, wherein the semiconductor integrated circuit device includes a detection circuit for detecting the input voltage and controls the control logic circuit in accordance with a detection result.